Amendments

In The Specification:

Please amend the specification as follows:

Page 6, replace the paragraph beginning on line 19 with the following rewritten paragraph:

It is desirable to adopt the standard cell system or full custom system as described above for the purpose of reducing the area of an IC chip. As has been practiced by the embedded array system in general, a single common mask used for the formation of each non-customized layer is designed and manufactured prior to (or in parallel with) the formation of a customized layer so that the TAT can be shortened.

Pages 6, replace the paragraph beginning on line 26 with the following rewritten paragraph:

In order to previously design and manufacture the common mask for the non-customized layer, the following two conditions must be met. The first condition is as follows: It is necessary to fix patterns for functional elements or devices such as transistors for constituting each non-customized layer and avoid changes in patterns after the design and fabrication of the mask are started. Further, the second condition is as follows: Interconnections in each wiring layer used as a customized layer are suitably formed in association with the non-customized layer so that desired functions are obtained. Namely, if basic gates (also called "basic cells") based on the gate array system are partially embedded in the IC designed by the standard cell system or full custom system, and the plurality of embedded basic gates are electrically connected to one another and utilized in combination so as to implement the desired functions, then the common mask used for the non-customized layer can be designed and fabricated prior to the formation of

the customized layer even in the case of the IC designed by the standard cell system or full custom system.

Page 7, replace the paragraph beginning on line 17 with the following rewritten paragraph:

A process for designing such an IC as to allow the common mask for the non-customized layer to be designed and fabricated prior to the formation of the customized layer, using the standard cell system or full custom system will next be explained.

Pages 7, replace the paragraph beginning on line 28 with the following rewritten paragraph:

Next, design resources based on the gate array system are blocked to effect layout design on the area having the potential of change in circuit. The layout of the entire IC is designed while the blocked design resources based on the gate array system are being captured by a CAD (Computer Aided Design) of the standard cell system or full custom system. Upon completion of the layout design of the entire IC, the design and fabrication of the common mask related to the non-customized layer is started.

Subt D5 Page 8, replace the paragraph beginning on line 8 with the following rewritten paragraph:

Thereafter, when the contents of the circuit is determined in the area having the potential of the change in circuit, each gate array block corresponding to a basic cell block is again laid out using the CAD of the gate array system. The design and fabrication of a circuit mask corresponding to each customized layer are started based on the re-laid out gate array block. C5 Incidentally, the gate array block whose circuit has been determined, is laid-out in a design based on the non-customized layer formed by the previously-designed and fabricated common mask. Namely, the gate array block preceding the determination of the circuit and the gate array block subsequent to the determination of the circuit are respectively made up of the same basic gate comprised of basic gates identical in number in both the vertical and horizontal directions.

Page 10, replace the paragraph beginning on line 4 with the following rewritten paragraph:

Since diffused layers, polysilicon layers, metal wiring layers, etc. are conventionally formed after the design and fabrication of the masks when the IC is designed by the standard cell system or full custom system, it normally took several months to complete the IC. On the other hand, according to the IC chip 1 in an embodiment of the present invention, it is possible to previously design and manufacture the common mask corresponding to the non-customized layer during a logic-simulation stage, for example. Further, the design work such as the logic simulation or the like is continuously performed in parallel with the design and fabrication of the common mask. Thereafter, when the corresponding circuit for the gate array block 34 has been determined, the layout of the gate array block 34 is designed again, and the circuit mask corresponding to a customized layer is designed fabricated.

Page 11, replace the paragraph beginning on line 1 with the following rewritten paragraph:

According to the IC chip 1 related to the embodiment of the present invention, when a circuit change occurs in the gate array block 34, the designer of the IC chip can cope with such a circuit change by redesigning only the gate array block 34 while the contents of the circuit of the non-customized layer is maintained. That is, only the circuit mask related to the gate array block 34 is changed in design. Thus, the circuit change of the gate array block 34 can be completed in a short period of time.